U.S. UTILITY Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10063737	05/09/2002	716	1	2825	Bowers

**APPLICANTS: Hsu Jimmy;

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
TAIWAN 91102057 02/06/2002 BB

PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☑ yes ☐ no
35 USC 119 conditions met ☑ yes ☐ no
Verified and Acknowledged Examiners's intials BB

ATTORNEY DOCKET NO
8727-US-PA

TITLE : Voltage reference circuit layout inside multi-layered substrate

U.S.DEPT. OF COMM./PAT.& TM-PTO-436L(Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED: Total Claims / Print Claim for O.G
ISSUE FEE: Amount Due / Date Paid		Primary Examiner	DRAWING: Sheets Drwg. / Figs.Drwg. / Print Fig.
☐ TERMINAL DISCLAIMER		PREPARED FOR ISSUE	Application Examiner

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